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10/663,098	09/15/2003	Tsvika Kurts	P17694	1638

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EXAMINER	
SURYAWANSHI, SURESH	
ART UNIT	**PAPER NUMBER**
2115	

DATE MAILED: 03/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/663,098	KURTS ET AL.	
	Examiner	Art Unit	
	Suresh K. Suryawanshi	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-41* is/are rejected.

7)☒ Claim(s) *13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/18/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-41 are presented for examination.

Claim Objections

2. Claim 13 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim, or amend the claim to place the claim in proper dependent form, or rewrite the claim in independent form.

Claim 13 recites that the apparatus claim 1 further comprising the peripheral set. However, claim 1 already recites for having the peripheral set. Therefore, claim 13 is improper as it does not further limit the subject matter of the previous claim 1.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claim 16 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 16 recites "the clock rate feedback unit comprises one of: a circuit within the clock generator; a circuit within the processor; and a circuit within a memory controller hub, said memory controller hub to couple with both the clock generator and the processor." But provided specification and figures disclose that the clock rate feedback unit is a separate circuit than disclosed a circuit within the clock generator and a circuit within the processor. The applicant could claim that it is a circuit within a memory controller hub as shown in figure 1. The examiner submits that it would require undue experimentation to make and use the claimed circuits.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-5, 7, 12, 14-15, 18-32, 35-36, and 38-41 are rejected under 35 U.S.C. 102(b) as being anticipated by Wilson et al (US Patent 6,385,735; hereinafter Wilson).

7. As per claim 1, Wilson discloses an apparatus comprising:

a memory element in a processor to supply a configured clock rate setting for use by a peripheral set [Fig. 1 and 2; col. 4, lines 8-12; a frequency limiting fuse that can be used by any peripheral set connected to the system motherboard];

an input element in the processor to receive a feedback clock rate setting from the peripheral set [Fig. 1 and 2; col. 3, lines 30-34, 52-55; frequency selecting circuit]; and

a comparison unit in the processor to compare the configured clock rate setting and the feedback clock rate setting to detect over-clocking of the processor [Fig. 1 and 2; col. 3, lines 30-34; col. 4, lines 45-63; comparator circuit].

8. As per claim 15, Wilson discloses an apparatus comprising:

a clock generator to generate a clock signal based on a clock rate setting [Fig. 1; col. 3, lines 5-6; a clock generation circuit], and said clock rate generator to provide the clock signal for use by a processor [Fig. 1; col. 3, lines 5-13], said processor having a configured clock rate setting [col. 5, lines 16-50; the processor manufacturer programs one or more of frequency limiting fuses to set the maximum clock frequency to prevent over clocking and remarking of processor]; and

a clock rate feedback unit to generate a feedback clock rate setting based on a clock rate of the clock signal [Fig. 1 and 2; col. 3, lines 32-34; col. 3, line 52 -- col. 4, line 7; frequency selecting circuit], and said clock rate feedback unit to provide the feedback clock rate back for use by the processor for comparison to the configured clock rate setting to detect over-clocking [Fig. 1 and 2; col. 30-34; col. 4, lines 45-63; comparator circuit].

9. As per claim 22, Wilson discloses a system comprising:

a processor [Fig. 1];

a clock generator to generate a clock signal for the processor based on a clock rate setting [Fig. 1 and 2]; and

a memory controller hub to supply a feedback clock rate setting based on a clock rate of the clock signal [Fig. 1 and 2; col. 3, lines 32-34; col. 3, line 52 -- col. 4, line 7; frequency selecting circuit; a memory controller hub is one of the many peripheral sets connected to the system motherboard];

said processor comprising a memory element to provide a configured clock rate setting for use by the clock generator [Fig. 1 and 2; col. 4, lines 8-12; a frequency limiting fuse], an input element to receive the feedback clock rate setting from the memory controller hub [Fig. 1 and 2; col. 3, lines 30-34, 52-55; frequency selecting circuit], and a comparison unit to compare the configured clock rate setting and the feedback clock rate setting to detect over-clocking of the processor [Fig. 1 and 2; col. 30-34; col. 4, lines 45-63; comparator circuit].

10. As per claim 25, Wilson discloses a method comprising:

providing a configured clock rate setting from a processor for use by a peripheral set [Fig. 1 and 2; col. 4, lines 8-12; a frequency limiting fuse that can be used by any peripheral set connected to the system motherboard];

receiving a feedback clock rate setting at the processor from the peripheral set [Fig. 1 and 2; col. 3, lines 30-34, 52-55; frequency selecting circuit]; and

comparing the configured clock rate setting and the feedback clock rate setting to detect over-clocking of the processor [Fig. 1 and 2; col. 30-34; col. 4, lines 45-63; comparator circuit].

11. As per claim 36, Wilson discloses a method comprising:

generating a clock signal at a peripheral set based on a clock rate setting [Fig. 1 and 2; col. 3, lines 5-6; a clock generation circuit; col. 4, lines 8-12; a frequency limiting fuse];

providing the clock signal from the peripheral set for use by a processor, said processor having a configured clock rate setting [Fig. 1 and 2; col. 3, lines 30-34, 52-55; frequency selecting circuit]; and

generating a feedback clock rate setting based on a clock rate of the clock signal for use by the processor for comparison to the configured clock rate setting to detect over-clocking [Fig. 1 and 2; col. 30-34; col. 4, lines 45-63; comparator circuit].

12. As per claim 39, Wilson discloses

providing a configured clock rate setting from a processor for use by a peripheral set [Fig. 1 and 2; col. 4, lines 8-12; a frequency limiting fuse that can be used by any peripheral set connected to the system motherboard];

receiving a feedback clock rate setting at the processor from the peripheral set [Fig. 1 and 2; col. 3, lines 30-34, 52-55; frequency selecting circuit]; and

comparing the configured clock rate setting and the feedback clock rate setting to detect over-clocking of the processor [Fig. 1 and 2; col. 30-34; col. 4, lines 45-63; comparator circuit].

13. As per claim 2, Wilson discloses that the memory element comprises at least one fuse [Fig. 2; col. 4, lines 8-12; frequency limiting fuses].

14. As per claim 3, Wilson discloses that the input element comprises at least one digital register [Fig. 1 and 2].

15. As per claims 4 and 23, Wilson discloses that a control unit in the processor to place the processor in a detected state if the comparison unit detects over-clocking [Fig. 2; col. 4, line 64 -- col. 5, line 15].

16. As per claim 5, Wilson discloses that a second memory element in the processor to store a detection enable setting [Fig. 2; col. 4, lines 45-63].

17. As per claims 7, 24 and 32, Wilson discloses that the detected state comprises one of a low frequency mode and a shut down mode [col. 5, lines 5-15].

18. As per claim 12, Wilson discloses that the configured clock rate setting and the feedback clock rate setting each comprise digital codes of at least one bit each, and wherein the comparison unit comprises a digital comparator [Fig. 2 and 5; col. 4, lines 45-63; both the configured clock setting and the feedback clock rate setting provide 4-bit digital values].

19. As per claim 14, Wilson discloses that the peripheral set comprises at least one of a clock generator, a memory, an input/output interface, a memory controller hub, and an input/output controller hub [Fig. 1; a motherboard of a computer system contains a clock generator, a memory, an input/output interface, a memory controller hub, and an input/output controller hub and more].

20. As per claim 18, Wilson discloses that the clock generator and the clock rate feedback unit comprise a peripheral set to couple with the processor [Fig. 1 and 2; motherboard].

21. As per claim 19, Wilson discloses that a memory element to store the clock rate setting during each reset of the processor [Fig. 2].

22. As per claim 20, Wilson discloses that a memory controller hub comprises at least one of the clock generator and the clock rate feedback unit; and a front side bus to couple the memory controller hub with the processor [Fig. 1].

23. As per claim 21, Wilson discloses that said memory controller hub is to supply the processor with a power-on-configuration signal during each reset of the processor, said power-on-configuration signal comprising the feedback clock rate setting [Fig. 1 and 2; col. 4, line 64 -- col. 5, line 4].

24. As per claim 26, Wilson discloses that comparing comprises determining if the feedback clock rate setting is higher than the configured clock rate [Fig. 2; col. 4, lines 45-63].

25. As per claim 27, Wilson discloses that configuring a memory element in the processor with the configured clock rate setting prior to providing the configured clock rate setting [col. 4, lines 8-14].

26. As per claim 28, Wilson discloses that configuring the memory element comprises blowing at least one fuse [col. 4, lines 8-14].

27. As per claim 29, Wilson discloses that receiving the feedback clock rate setting comprises storing the feedback clock rate setting to a memory element in the processor for each reset of the processor [Fig. 1 and 2; col. 2, lines 53-62].

28. As per claims 30 and 40, Wilson discloses that placing the processor in a detected state if over-clocking is detected [Fig. 2; col. 4, lines 45-63].

29. As per claim 31, Wilson discloses asserting an enforce signal and a detecting signal and initiating the detected state [Fig. 2; col. 4, line 45 -- col. 5, line 50].

30. As per claim 38, Wilson discloses storing the clock rate setting during each reset of the processor [col. 2, lines 53-62; col. 4, line 64 -- col. 5, line 4].

31. As per claim 35, Wilson discloses receiving a power-on-configuration signal [col. 2, lines 58-62; col. 4, line 64 -- col. 5, line 4].

32. As per claim 41, Wilson discloses

generating a clock signal at the peripheral set based on a clock rate setting [Fig. 1; processor clock frequency selection signal];

providing the clock signal from the peripheral set for use by the processor [Fig. 1 and 2]; and

generating the feedback clock rate setting based on a clock rate of the clock signal [Fig. 1 and 2; frequency selecting circuit].

Claim Rejections - 35 USC § 103

33. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

34. Claim 6, 17 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wilson et al (US Patent 6,385,735; hereinafter Wilson).

35. As per claim 6, Wilson discloses the invention substantially. Wilson does not disclose that the second memory to store the detection enable setting comprises a fuse. Wilson uses a register. However, Wilson expressly discloses using frequency limiting fuses and frequency selecting fuses [Fig. 2]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize a fuse instead a register to store the detection enable setting. Moreover, a use of fuse will definitely put down a computer system in a permanent shut down mode until the fuse is replaced. Thus, discouraging over clocking in a computer system.

36. As per claims 17 and 37, Wilson discloses the invention substantially. Wilson does not expressly disclose that the clock rate feedback unit comprises one of a frequency measurement circuit to measure a frequency of the clock signal and a register to store a code indicating a current clock rate setting of the clock generator. However, as shown in Fig. 2, comparator circuit needs to know about the current clock rate of the clock generator and it is fed through the frequency selecting circuit 40. Thus, there may be a frequency measurement circuit to measure

the frequency of the clock signal from the clock generator and a register to store a code indicating it [4-bit digital value; col. 4, lines 45-63]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize a frequency measurement circuit and store the measurement in a memory location accessible by the comparator.

37. Claims 8 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wilson et al (US Patent 6,385,735; hereinafter Wilson) in view of Pollock et al (US Patent 6,691,242; hereinafter Pollock).

38. As per claims 8 and 33, Wilson discloses the invention substantially. Wilson does not disclose outputting an over-clocking detection signal from the processor. However, Pollock clearly discloses warning a user of the computer system if the processor of the system is running at a greater speed than recommended under warranty [Fig. 1 and 3]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as both are directed for detecting if a processor is being over clocked. Moreover, indication of such a warning will definitely help a user to know that the processor of the computer system has been over clocked.

39. Claims 9-11 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wilson et al (US Patent 6,385,735; hereinafter Wilson) in view of Watabe et al (US Patent 6,073,249; hereinafter Watabe).

40. As per claims 9-11 and 34, Wilson discloses the invention substantially. Wilson does not disclose expressly about use of a tri-state unit and a logic AND. But a routineer in the art would know about a tri-state unit and a logic AND as these are well known for their use. However, Watabe clearly discloses use of a tri-state unit and a logic AND [Fig. 2, 4 and 5; tri-state circuit 24 and logic AND 36]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as both are directed to an information processing system and handling a failure in the information processing system. Moreover, a routineer would use well-known circuits in the art to keep both cost of the system and time to produce at minimum.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suresh K. Suryawanshi whose telephone number is 571-272-3668. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sks
February 16, 2006

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